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### On-wafer calibration techniques for giga-hertz CMOS ...

techniques. When the amount of impairments on the system are  $-4 -2 0 2 4 \times 10^{-4}$   $-4 -2 0 2 4 \times 10^{-4}$  Figure 2. The dashed lines are the decision boundaries for symbols, circles are the ideal symbol locations. known, they can be analytically calibrated by modeling quadrature imbalance and non-linear compression behaviors.

### Digital Calibration of RF Transceivers for I-Q Imbalances ...

The design was fabricated in a 0.35- $\mu$ m CMOS process and dissipates 160 mW from a 3-V supply during on-line calibration, and 95 mW during normal receiving. The die area is 4 mm<sup>2</sup>. View

### A Low-Complexity I/Q Imbalance Calibration Method for ...

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### IQ calibration techniques for CMOS radio transceivers ...

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IQ mixer, an analog component for which calibration is necessary to achieve optimal performance. In this paper, we introduce techniques originally developed for wireless communication applications to calibrate upconversion and downconversion mixers. A Kalman filter together with a controllable carrier frequency offset calibrates both mixers

**IQ Mixer Calibration for Superconducting Circuits**

CMOS PLL calibration techniques Abstract: The article discusses auto calibration of phase lock loops (PLLs), particularly when used as frequency synthesizers in fully integrated radios targeting future generations of broadband wireless applications.

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